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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/920,062	08/01/2001	Eun Youp Kong	5649-888	4437

20792 7590 11/07/2003

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EXAMINER
TRAN, LONG K

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,062	KONG ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *19-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *102203* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Election/Restrictions

1. Applicant's election without traverse of **Invention I**, claims **1 – 18**, filed on August 22, 2003 is acknowledged.

2. Claims **19 – 21** have been withdrawn

3. Claims **22 – 28** have been cancelled.

4. Claims **1 – 18** are presented for examination.

Priority

5. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on August 1, 2001.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **1 – 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over DasGupta et al. (US Patent No. 4,503,386).

Regarding claims **1, 3, 4, 5, 6, 7, 9, 10**, DasGupta et al. disclose a multi-chip memory device, comprising: integrated circuit memory chips (figs. 9 and 10,1 – 4), each of which includes a plurality of corresponding address, data, control signal and clock; a common package that encapsulates the four integrated circuit memory chips and that includes a plurality of external terminals (fig. 3, blocks A & B; col. 14, lines 1+); and an

internal connection circuit in the common package that is configured to connect at least one of the corresponding control signal pads of each of the integrated circuit memory chips to separate ones of the plurality of external terminals (figs 9 and 10) and the integrated circuit memory chips are encapsulated in the common package (figs 9 & 10, col. 4 lines 6 – 20). DasGupta et al. do not explicitly teach address, data and control signal pad; and to allow independent external control of each of the integrated circuit memory chips. However, the module or chip package (fig. 10) is identical to that of (fig.9) of the claimed invention. Therefore, it is inherent that the package of DasGupta et al. will have all limitations and fixtures as the package of the claimed invention.

Regarding claim **2**, DasGupta et al. disclose the claimed invention of claim 1 except for at least two integrated circuit memory chips are identical. However, It would have been obvious to one having ordinary skill in the art at the time the invention was made to design the memory package of DasGupta et al. with at least two identical integrated circuit memory chip, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

8. Claims **2** and **8** are rejected under 35 U.S.C. 103(a) as being unpatentable over DasGupta et al. (US Patent No. 4,503,386) in view of Yamasaki (US Patent No. 6,433,422).

Regarding claims **2** and **8**, DasGupta et al. disclose the claimed invention of claim 1 but fail to explicitly teach at least two integrated circuit memory chip are identical; and a memory module substrate including first and second opposing surfaces, wherein the multi-chip memory device is a first multi-chip memory device and is on the first surface, and in

further combination with a second multi-chip memory device on the second surface. However, Yamasaki discloses a small high-density packaging comprising a pair of small CSPs (fig. 6,11 and 12; col. 3, lines 66+ and col. 4, lines 1+) mounted on both side of the substrate (fig. 6, 25). However, It would have been obvious to one having ordinary skill in the art at the time the invention was made to design the memory package of DasGupta et al. with at least two identical integrated circuit memory chip; and a memory module substrate including first and second opposing surfaces, wherein the multi-chip memory device is a first multi-chip memory device and is on the first surface, and in further combination with a second multi-chip memory device on the second surface, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Regarding claims **11, 12, 13, 14, 15, 16, 17** and **18** DasGupta et al. disclose a multi-chip memory device, comprising: integrated circuit memory chips (figs. 9 and 10,1 – 4), each of which includes a plurality of corresponding address, data, control signal and clock; a common package that encapsulates the four integrated circuit memory chips and that includes a plurality of external terminals (fig. 3, blocks A & B; col. 14, lines 1+); and an internal connection circuit in the common package that is configured to connect at least one of the corresponding control signal pads of each of the integrated circuit memory chips to separate ones of the plurality of external terminals (figs 9 and 10) and the integrated circuit memory chips are encapsulated in the common package (figs 9 & 10, col. 4 lines 6 – 20). DasGupta et al. do not explicitly teach address, data and control signal pad; and to allow independent external control of each of the

integrated circuit memory chips. However, the module or chip package (fig. 10) is identical to that of (fig.9) of the claimed invention. Therefore, it is inherent that the package of DasGupta et al. will have all limitations and fixtures as the package of the claimed invention.

In addition, DasGupta et al. do not explicitly teach at least two integrated circuit memory chip are identical; and a memory module substrate including first and second opposing surfaces, wherein the multi-chip memory device is a first multi-chip memory device and is on the first surface, and in further combination with a second multi-chip memory device on the second surface. However, Yamasaki discloses a small high-density packaging comprising a pair of small CSPs (fig. 6,11 and 12; col. 3, lines 66+ and col. 4, lines 1+) mounted on both side of the substrate (fig. 6, 25). However, It would have been obvious to one having ordinary skill in the art at the time the invention was made to design the memory package of DasGupta et al. with at least two identical integrated circuit memory chip; and a memory module substrate including first and second opposing surfaces, wherein the multi-chip memory device is a first multi-chip memory device and is on the first surface, and in further combination with a second multi-chip memory device on the second surface, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Osaka et al. (US Patent No. 6,438,012), Goel et al. (US Patent

No. 4,494,066), McMahon (US Patent No. 4,441,075) and Russel et al (US Patent No. 5,637,828)) discloses a memory device similar to that of DasGupta et al. (US Patent No. 4,503,386) and Yamasaki (US Patent No. 6,433,422).

10. A shortened statutory period for response to this action is set to expire e (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 703-305-5482. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Long Tran

October 22, 2003

HOAI HO
PRIMARY EXAMINER